Application No.: 09/940,324
Response dated: March 27, 2006
Reply to Final Office Action dated: December 27, 2005

REMARKS/ARGUMENTS

Claims 1-17 are pending in the application.

1. Claim Rejections under 35 U.S.C. §102

Claims 9-15 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,751,705 to Solomon et al. Applicants respectfully disagree.

Claim 9 recites a plurality of client ports on an I/O cache-coherent device. The Examiner has asserted that Solomon teaches the recited I/O cache-coherent device, referring to a transaction handler 26 shown in Fig. 2 of Solomon. At the same time, the Examiner has asserted that Solomon teaches the recited plurality of client ports on an I/O cache-coherence device, referring to processor bridges 120 and 220 shown in Fig. 15, and a DRAM interface 1600 shown in Fig. 2 of Solomon.

However, as shown in Fig. 2 of Solomon, the transaction handler 26 is in a processor bridge 20 and is a part of the processor bridge 20. The processor bridge 20 could not possibly be a client port on the transaction handler 26. Similarly, elements 120 and 220 in Solomon, which are also processor bridges, could not be a client port on the transaction handler 26 either. Thus, it is incorrect for the Examiner to read the recited I/O cache-coherent device on Solomon's transaction handler 26, while reading the recited client ports on the I/O cache-coherent device on Solomon's processor bridges 120 and 220.

Even assuming, *arguendo*, that the Examiner could reasonably read the recited client port on Solomon's DRAM interface 1600, Solomon fails to teach the invention of claim 9. First, as Applicants presented before, the processor bridge 20 includes *only one* DRAM interface 1600. Solomon fails to teach *a plurality of* client ports on an I/O cache-coherency device. Further, in Solomon, a processor bridge 20 includes *one* DRAM interface 1600 connected to *one* bridge cache 112 (Solomon, Fig. 2 and col. 5, lines 5-15). Thus, it is impossible for Solomon to teach *a plurality of* sub-unit caches, each assigned to one of the *plurality of* client ports on an I/O cache-coherent device.

Although Solomon may have a plurality of bridge caches 112, each of the bridge caches 112 is connected to only one processor bridge, and each pair of bridge cache 112 and its DRAM interface 1600 belongs to one separate processor bridge. Solomon does not teach any single device which has a plurality of DRAM interfaces 1600, each accessing one of a plurality of sub-unit caches. Thus, Solomon fails to teach *a plurality* of sub-unit caches, each assigned to one of the *plurality of* client ports on an I/O cache-coherent device.

Accordingly, Applicants respectfully resubmit that claims 9-17 are patentable over Solomon.

2. Claim Rejections under 35 U.S.C. §103

A. Claims 1-8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Solomon in view of Yasuda et al. (Yasuda) U.S. Patent 6,636,926.

The Examiner has argued that Solomon teaches the recited a plurality of sub-unit caches,

each coupled to one of a plurality of client ports and assigned to one of a plurality of port components. Applicants respectfully disagree.

The Examiner has asserted that Solomon's processors 118 and 218 teach the recited port components, and Solomon's L2 caches 112 teach the recited sub-unit caches. However, in Solomon, each processor 118 and 119 includes a Level 0 cache 110 and a Level 1 cache 111, and bridge cache 112 becomes a Level 2 cache for processors 118 *and* 119 (Fig. 15, col. 21, lines 1-5). Thus, the L2 cache 112 in Solomon is accessed by *both* processor 118 and processor 119. Solomon fails to teach assigning one sub-unit cache to *one of a plurality of* processors. Accordingly, Applicants resubmit that Solomon fails to teach or suggest a plurality of sub-unit caches, each coupled to one of said plurality of client ports and assigned to *one of a plurality of* port components.

The Examiner has agreed that Solomon fails to teach a coherency engine coupled to a plurality of sub-unit caches, but has asserted that Yasuda provides this feature, referring to a cache coherence control circuit 330. Applicants respectfully disagree.

Applicants argued in the Response dated November 14, 2005 that Yasuda fails to compensate for Solomon's deficiency. Yasuda discloses a shared memory multiprocessor performing cache coherence control. In Yasuda, the cache coherence control circuit 330 works with the access request holding unit 321 to decide whether to transmit a cache coherence control request. There is nothing in Yasuda supporting the Examiner's argument that the cache coherence control circuit 330 is coupled to a plurality of sub-unit caches. Thus, even if a skilled

artisan were to combine Solomon and Yasuda, the combination would not result in the invention of claim 1.

The Examiner maintained his rejection without explaining why he did not agree with Applicants arguments regarding Yasuda. For now, Applicants respectfully resubmit that claims 1-8 are patentable over the combination of Solomon and Yasuda.

B. Claims 16-17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Solomon in view of Witt et al (Witt) U.S. Patent 6,202,139.

As discussed above, Solomon fails to teach a plurality of client ports on an input/output cache-coherent device, and fails to teach a plurality of sub-unit caches, each assigned to one of the plurality of client ports on the I/O cache-coherent device.

Witt fails to supply any deficiencies of Solomon. Witt discloses a pipelined data cache, and states:

> Generally speaking, microprocessor 10 employs a multiported data cache 14, allowing for multiple memory operations to be performed in parallel. The array within data cache 14 is physically single ported, but data cache 14 is pipelined into multiple stages. The pipeline within data cache 14 is operated at a clock frequency which is a multiple of the clock frequency at which the remainder of microprocessor 10 operates.

(Witt, col. 4, lines 42-45).

Witt does not teach a plurality of sub-unit caches, each assigned to one of a plurality of client ports on an input/output cache-coherent device as recited in claim 9 either. Applicants

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respectfully resubmit that claims 16 and 17 are patentable over Solomon and Witt for this additional reason as well.

For all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to the deposit account of Kenyon & Kenyon, deposit account no. **11-0600.**

Respectfully submitted,

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